**Xilinx ISE Lab 4\_K-Map**

***General Statement:*** Implement function **F(A,B,C,D) = Sum(0,1,7,13,15) +Don’t Cares(2,6,8,9,10)** by onlyusing **two-level logic**. Thus, you are to draw the circuit using the **Xilinx ISE Schematic Editor**, and then simulate it using the **Xilinx ISE Simulator**. You are to get a printout of the Simulation results (i.e. the timing diagram).

Your completed report should include:

**(1)** This cover sheet, followed by

**(2)** Function table for the above function

**(3)** K-map simplification

**(4)** A printout of the circuit via **Schematic** Editor, followed by

**(5)** A printout of the timing diagram via Xilinx Simulator

(6) Verilog test bench code (you can modify the tutorial to reflect this one\_this time you have four inputs and one output)

Once your design is verified using the Xilinx simulator, you are to get (1) a printout of the actual circuit from the Schematic Editor and (2) a printout of the simulation waveforms.

initial begin

// test case 0

A = 0;

B = 0;

C = 0;

D = 0;

#10;// Wait 10 time units

// test case 1

A = 0;

B = 0;

C = 0;

D = 1;

#10;// Wait 10 time units

//add more cases here

$stop;

end